# METHOD OF ENLARGING CONTACT AREA OF A GATE ELECTRODE, SEMICONDUCTOR DEVICE HAVING A SURFACE-ENLARGED GATE ELECTRODE, AND METHOD OF MANUFACTURING THE SAME

## BACKGROUND OF THE INVENTION

1. Field of the Invention

**[0005]** The present invention relates to a semiconductor device having a mushroom- or T-shaped gate electrode, and to a method of fabricating the mushroom or T-shaped gate electrode. More specifically, the present invention relates to a semiconductor device having a gate electrode whose upper surface is relatively large so as to accommodate a metal silicide, and to a method of fabricating a gate electrode wherein the upper surface of the gate electrode is enlarged.

2. Description of the Related Art

**[0010]** Recent sub-micron integrated circuit technology aims at continuously reducing the line width and contact area of the semiconductor device, whereby the length of the gate lines of integrated circuits is continuously decreasing. In general, shortening the gate line increases the electrical resistance of the gate line (hereinafter, referred to as line resistance), resulting in a corresponding reduction in the operating speed of the gate line. That is, the operating speed in an integrated circuit is mainly dependent on a delay time, and the line resistance and parasitic capacitance between the gate lines have a decisive effect on the delay time. Accordingly, increases in the operating speed of the integrated circuit must be achieved by reducing the line resistance or reducing the parasitic capacitance by widening the space between the gate lines.

**[0015]** Most of the technology has focused on decreasing the line resistance to

improve the operating speed of the integrated circuit because the alternative solution of widening the space between the gate lines runs counter to the aim of achieving a high degree of integration of the integrated circuit. A recent technological trend involves the use of a polycide layer to minimize the line resistance. Specifically, a silicide layer including a metal having a high melting point is coated on an upper portion of a gate electrode formed of polysilicon, and the silicide layer is incorporated with the gate electrode by a heat treatment to form the polycide layer.

**[0020]** However, when the line width of the integrated circuit is less than 0.13 μm, the length and width of the gate electrode are correspondingly small, and the surface area of the gate electrode is also extremely small. Accordingly, the contact area between the gate electrode and the metal used to form the silicide layer is so small that the silicide layer is not sufficiently incorporated into the gate electrode by the heat treatment. That is, when the line width is less than 0.13 μm, the resistance of the polycide layer on the gate electrode is unstable and hence, the polycide layer does not reduce the electrical resistance at the gate electrode.

**[0025]** Delay time also results from the parasitic capacitance generated in a region of overlap between the gate electrode and the substrate. In the fabricating of semiconductor devices, the gate electrode is first formed of polysilicon on the substrate such that a dimension of the gate electrode conforms to the length of a channel layer under the gate electrode, and then source/drain electrodes are subsequently formed through an ion implantation process. A plurality of dopants are injected into an active region of the substrate to form the source/drain electrodes, and a heat treatment is performed for stabilizing the substrate. However, the dopants diffuse to the edge portion of the gate electrode due to the heat. Accordingly, the source and drain electrodes extend to locations beneath the gate electrode at both

edge portions thereof. Accordingly, the channel layer is shortened by an amount corresponding to the amount of overlap between the gate electrode and the source/drain electrodes (short channel effect). The overlapping portion acts as a parasitic capacitor between the gate electrode and the substrate because the overlapping portion is electrically non-conductive. When an electrical current is applied to the source electrode, the parasitic capacitor is first charged and then, the current passes into the drain electrode through the channel layer. Therefore, a time delay is produced according to the time it takes to charge the parasitic capacitor. That is, the parasitic capacitance (hereinafter referred to as "overlay parasitic capacitance") reduces the operating speed of the integrated circuit. The operating speed is also reduced due to an overlay parasitic capacitor created as the result of a halo ion implantation process for preventing the diffusion of the source/drain dopants.

**[0030]** Ways to improve the resistance characteristic of the polycide gate electrode have been researched in connection with the fabricating of semiconductor devices having a design rule of less than 0.1 μm. For example, U.S. Patent No. 6,169,017 (issued to Tong-Hsin Lee) discloses a technique of enlarging the upper surface of the gate electrode with which the silicide layer is to contact, whereupon the gate electrode is T-shaped or mushroom-shaped. Furthermore, Japanese Laid-Open Patent Publication No. 2000-36594 discloses a method of fabricating a polycide gate electrode, wherein polysilicon is twice deposited on a substrate such that an upper portion of the gate electrode is larger than the lower portion thereof. However, these techniques each fail to prevent the occurrence of a time delay due to the overlay parasitic capacitance between the gate electrode and substrate.

## SUMMARY OF THE INVENTION

**[0035]** Accordingly, an object of the present invention is to provide a method of forming a gate electrode having a stable polycide layer and yet wherein overlay parasitic capacitance between the gate electrode and the substrate is minimal.

**[0040]** Another object of the present invention is to provide a highly integrated semiconductor device having a high operating speed, and to provide a method of fabricating the same.

**[0045]** Likewise, a more specific object of the present invention is to provide a semiconductor device whose gate electrode offers little resistance and yet gives rise to hardly any parasitic capacitance.

**[0050]** According to one aspect of the present invention, a method of forming a gate structure in a semiconductor device comprises a) forming a first insulating layer on a semiconductor substrate, forming a layer of conductive material on the first insulating layer, and patterning the first conductive layer to form at least one gate pattern, b) forming a second insulating layer on the gate pattern and substrate, c) reducing the thickness of the second insulating layer until the upper surface thereof becomes situated beneath the level of the upper surface of the gate pattern, d) forming a second conductive layer over the resultant structure, e) selectively removing portions of the second conductive layer such that a spacer of the conductive material is formed at both sides of an upper portion of the gate pattern, and f) subsequently removing portions of the second insulating layer other than those located beneath the spacer.

**[0055]** The thickness of the second insulating layer is preferably reduced by a chemical mechanical polishing (CMP) process followed by a wet-etch process. After the second conductive layer is formed on the second insulating layer and the gate

pattern, the second conductive layer is selectively etched by an anisotropic etching process. As a result, the spacer formed by the conductive material at both sides of the upper portion of the gate pattern enlarges the surface area of the gate pattern.

**[0060]** According to another aspect of the present invention, a method of forming a semiconductor device comprises a) forming a first insulating layer on a semiconductor substrate, forming a layer of conductive material on the first insulating layer, and patterning the first conductive layer to form at least one gate pattern, b) forming a second insulating layer on the gate pattern and substrate, c) reducing the thickness of the second insulating layer until the upper surface thereof becomes situated beneath the level of the upper surface of the gate pattern, d) forming a second conductive layer over the resultant structure, e) selectively removing portions of the second conductive layer such that a first spacer of the conductive material is formed at both sides of an upper portion of the gate pattern, f) subsequently removing portions of the second insulating layer other than those located beneath the spacer, g) implanting ions at a relatively low concentration into the substrate at the sides of the gate pattern to form a lightly-doped source/drain region, h) forming a fourth insulating layer over the resultant structure, i) selectively removing portions of the fourth insulating layer to form a second spacer at the sides of the gate pattern, j) subsequently implanting ions at a relatively heavy concentration into the substrate at the sides of the gate pattern to form a heavily-doped source/drain region, k) subsequently heat-treating the substrate to chemically bond the dopants to the substrate, and m) forming a third conductive layer on the gate pattern and first spacer.

**[0065]** In addition, portions of the first insulating layer may be etched away with those of the second insulating layer (f) such that the surface of the substrate is exposed. In this case, a third insulating layer is formed over the entire surface of the

substrate and on the enlarged gate pattern. Subsequently, the lightly concentrated ions are implanted into the substrate (g) using the gate pattern as a mask.

**[0070]** Preferably, the fourth insulating layer is formed (h) on the third insulating layer using a CVD or a PVD process, and is subsequently selectively etched (i) using an anisotropic etching process. The heavily concentrated of ions are implanted into the substrate using the enlarged gate pattern and the second spacer as masks.

**[0075]** According to still another aspect of the present invention, a semiconductor device comprises a) a semiconductor substrate, b) a gate insulating layer disposed on the substrate, c) a T- or mushroom-shaped gate electrode including a man body disposed on the gate insulating layer and wings extending laterally from an upper portion of the main body, e) a capacitance preventative layer of insulating material disposed under the wings of the T- or mushroom-shaped gate electrode, d) a discrete spacer disposed at both sides of the gate electrode laterally of the capacitance preventative layer and, e) a source electrode and a drain electrode defined at opposite sides of the gate electrode.

**[0080]** The semiconductor substrate includes an active region defined by an isolation structure such as a shallow trench isolation structure. The gate-insulating layer is coated on the substrate in the active region. The capacitance preventative layer contacts the main body of the gate electrode and gate insulating layer.

**[0085]** Preferably, the main body and wings of the gate electrode comprise polysilicon, and the capacitance preventative layer is a low-temperature oxide (LTO). In addition, the semiconductor device of the present invention may further comprise an anti-diffusion layer for preventing ion dopants in the source/drain region of the substrate from diffusing into a channel region located beneath the gate electrode. The gate electrode preferably also comprises a metal silicide layer on the main body

and wings thereof to thereby reduce the electrical resistance of the gate electrode. The metal silicide layer may also be disposed on the source/drain electrode to thereby to reduce the electrical resistance thereof.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0090]** The above and other objects, features and advantages of the present invention will become more readily apparent by referring to the following detailed description of the preferred embodiments thereof made in conjunction with the accompanying drawings, in which:

FIGS. 1A to 1M are cross-sectional views of a substrate, illustrating a method of manufacturing a semiconductor device according to the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0095]** The present invention now will be described more fully hereinafter with reference to the accompanying drawings.

**[0100]** Referring first to FIG. 1A, at least one gate pattern 14 is formed on a semiconductor substrate 10 as follows. The substrate 10 is coated with a first insulating layer 12, i.e., a gate insulating layer, and then the substrate 10 is coated with a first layer (not shown) of conductive material. Next, the first conductive layer is patterned to thereby form the gate pattern 14 on the substrate 10. Therefore, the gate pattern 14 is electrically insulated from the substrate 10 by the first insulating layer 12. A plurality of transistors are disposed on the substrate 10, and are electrically isolated from each other by an isolation structure 13. The isolation structure 13 defines an active region 11 of the substrate 10 in which the transistors operate. Current cannot pass through the isolation structure 13, which constitutes a field region or a non-

active region of a substrate, so that the active region 11 is electrically isolated from an adjacent active region. The isolation structure 13 is formed by a shallow trench isolation process, for example.

**[0105]** The first insulating layer may be a layer of silicon dioxide ($SiO_2$). The gate pattern 14 may comprise polysilicon. The polysilicon, from which the gate pattern 14 is formed, may be deposited on the substrate using a conventional deposition process.

**[0110]** Referring to FIG. 1B, a second insulating layer 16 is formed over the entire surface of the substrate 10. Accordingly, the second insulating layer 16 covers the gate pattern 14 and the surface of the substrate 10 in the active region 11. As an example, the second insulating layer 16 may be a low temperature oxide layer (hereinafter, referred to as an LTO layer), deposited to a thickness of about 3000 Å using a chemical vapor deposition (CVD) process or a plasma-CVD process.

**[0115]** Then, as shown in FIG. 1C, the second insulating layer 16 is planarized by a chemical mechanical polishing (CMP) process to reduce the thickness of the second insulating layer 16 until the upper surface thereof is situated about 700 Å over the upper surface of the gate pattern 14. Subsequently, the planarized second insulating layer 16a is etched using a wet-etching process to reduce the thickness thereof to about 900 Å from the upper surface of the insulating layer 12, as shown in FIG. 1D. As an example, the wet-etching process uses limulus amoebocyte lysate (LAL) solution as an etchant.

**[0120]** Referring to FIG. 1E, a second conductive layer 18 is formed over the entire surface of the substrate 10, so that the second conductive layer 18 covers an upper surface of the second insulating layer 16b and the gate pattern 14. The second conductive layer 18 comprises a polysilicon layer deposited, for example, to a

thickness of from about 300 Å to about 500 Å using a CVD process. The material of the second conductive layer 18 may vary, though, in accordance with the material of the gate pattern 14. Also, the surface of the second insulating layer 16b may be rinsed before the second conductive layer 18 is formed, to thereby remove residuals of the wet etching process. An aqueous detergent solution that is environmentally-friendly may be used to rinse the second insulating layer 16b.

**[0125]** Referring to FIG. 1F, the second conductive layer 18 is anisotropically etched by a dry etching process, thereby forming a first spacer 19 on an upper side portion of the gate pattern 14. Therefore, the effective surface area of the top of the gate pattern 14 is enlarged by the first spacer 19. Hereinafter, the gate pattern 14 and first spacer 19 will be collectively referred to as a surface-enlarged gate pattern and, more specifically, as a surface-enlarged gate poly when the surface-enlarged gate pattern comprises polysilicon. It should be clear, then, that the surface-enlarged gate poly provides a relatively large contact area for the silicide metal, whereby the polycide is sure to have the desired resistive characteristic.

**[0130]** Referring to FIG. 1G, the second insulating layer 16b is removed by a dry etching process using the surface-enlarged gate pattern as an etching mask so that only a portion of the second insulating layer 16c remains as interposed between the first spacer 19 and the first insulating layer 12 at the bottom portion of the gate pattern 14. The remaining second insulating layer 16c ensures that ions implanted during an ion implantation process for forming source and drain electrodes remain as far away from the gate pattern 14 as possible. That is, the remaining second insulating layer 16c prevents the dopants for forming the source and drain electrodes from diffusing to a portion of the substrate 10 under the gate pattern 14.

**[0135]** Also, as shown in FIG. 1G, the first insulating layer 12 is removed together

with the second insulating layer 16b. In fact, maintaining the first insulating layer 12 is expensive and difficult in view of the fact that the first insulating layer 12 is thinner than the targeted second insulating layer 16b. However, the first insulating layer 12 does not have to be removed along with the etched second insulating layer 16b, especially when the efficiency of the etching process does not depend on the removal of the first insulating layer 12.

**[0140]** Referring to FIG. 1H, a third insulating layer 20 is formed over the entire surface of the substrate 10. The third insulating layer 20 may be an oxide layer so as to function similarly to the first insulating layer 12. The oxide of the third insulating layer 20 grows inwardly rather than outwardly on the surface-enlarged gate poly because the oxide has a tendency to grow downwardly rather than upwardly on a silicide layer. The oxide layer 20 grows on the substrate 10 to the same height of the first insulating layer 12 because the third insulating layer 20 comprises the same material of the first insulating layer 12.

**[0145]** Referring to FIG. 1I, a diffusion-preventing layer 22a is formed by implanting diffusion-preventing ions under the gate electrode. The diffusion-preventing ions are for preventing dopants, subsequently implanted for forming the source and drain electrodes, from diffusing to the channel region under the gate electrode. To this end, the diffusion-preventing ions are implanted at a predetermined angle with respect to the surface of the substrate 10. As an example, the diffusion-preventing ions are implanted to the left of the surface-enlarged gate poly at an angle in a range of about 30° to about 45° clockwise with respect to the surface of the substrate 10, and are also implanted to the right of the surface-enlarged gate poly at an angle in a range of about 30° to about 45° counterclockwise with respect to the surface. The diffusion-preventing ions may be ions of germanium (Ge), phosphor (P),

silicon (Si), and indium (In).

**[0150]** Next, using the surface-enlarged gate poly as a mask, the dopants for forming the source/drain electrodes are implanted substantially at a right angle with respect to the surface of the substrate 10. Accordingly, a source/drain region is formed on each side of the surface-enlarged gate poly by the ion implantation process. The dopants include elements of group III or ï of the periodic table. In particular, the dopants are implanted at a low density near the gate electrode, thereby forming a lightly doped source/drain region 22b, to thereby minimize the chances for creating a short channel effect and overlay parasitic capacitance. Also, an optional extension process may be performed on the source/drain region for ensuring a more satisfactory flow of electrons toward the channel region.

**[0155]** Referring to FIG. 1J, a fourth insulating layer 23 is formed on the substrate 10 and thus, the third insulating layer 20 and the surface-enlarged gate poly are covered with the fourth insulating layer 23. The fourth insulating layer 23 may be a silicon nitride ($Si_3N_4$) layer formed on the substrate using a conventional CVD or PVD process. As shown in FIG. 1K, the fourth insulating layer 23 is selectively dry etched so that a second spacer 24 is formed at both sides of a lower portion of the surface-enlarged gate poly.

**[0160]** Referring to FIG. 1L, dopants for forming a source/drain region are implanted at a high density using the surface-enlarged gate poly and second spacer 24 as masks. The heavily doped source/drain region 26 is formed beneath the third insulating layer 20 to the side of the second spacer 24.

**[0165]** Subsequently, the substrate is heat-treated so that the dopants are chemically bonded to the substrate with sufficient stability. During the heat treatment, the dopants used to form a source/drain region usually diffuse toward the gate

electrode. However, according to the present invention, the dopants hardly reach the gate electrode because the implanted dopants are spaced from sidewalls of the gate electrode by an amount corresponding to the thickness of the remaining second insulating layer and the second spacer. Accordingly, parasitic capacitance is minimized and hence, the resultant semiconductor device does not operate with a long time delay.

**[0170]** In particular, the thickness of the second insulating layer 16c is dependent on the desired thickness of the second conductive layer 18. Moreover, some overlay parasitic capacitance is allowed for in the designing of the integrated circuit. However, the amount of overlay parasitic capacitance can not be predetermined because many factors influence the diffusion of the dopants, i.e., too much uncertainty is associated with the diffusion of the dopants. In any case, the remaining second insulating layer 16c of the present invention can diminish the uncertainty associated with the diffusion of the dopants. Specifically, the overlay parasitic capacitance will hardly have an influence on the functional characteristics of the device when the remaining second insulating layer 16c is formed to a sufficient thickness. That is, the thickness of the remaining second insulating layer 16c corresponds to a factor by which the effect of the overlay parasitic capacitance on the operation of the device is mitigated. In this respect, the thickness of the remaining second insulating layer 16c can be based just on the deposition thickness of the second conductive layer 18, and can be easily regulated during the manufacturing process.

**[0175]** Next, as shown in FIG. 1M, a silicide process for improving the resistance characteristic of the semiconductor device is performed. More specifically, the third insulating layer 20 is selectively etched, and a portion of the substrate 10 corresponding to the source/drain region (hereinafter, referred to as source/drain

substrate) is exposed. Then, a silicide layer is formed on the upper surface of the surface-enlarged gate poly and on the source/drain substrate, and a heat treatment is performed. As an example, the silicide layer is a refractory metal silicide layer comprising a metal such as cobalt (Co), tungsten (W) or titanium (Ti). As a result, the line resistance of the surface-enlarged gate poly and contact resistance of the source/drain resistance are reduced and, in turn, the operating speed of the semiconductor device is improved.

**[0180]** Finally, note, although the method of the present invention has been described above in connection with the manufacturing of a MOS-FET, the method of the present invention may also be applied to the manufacturing of a complementary MOS-FET as would be readily apparent to those of the ordinary skill in the art.

**[0185]** According to the present invention, as described above, wings in the form of a spacer are formed on both sides of an upper portion of the gate electrode. Thus, the wings enlarge the surface area of the exposed conductive material. Therefore, a silicide layer can make stable contact with the gate electrode, and a polycide layer can not reduce the electrical resistance at the gate electrode even when the gate length is on a sub-micron scale. In addition, an insulating layer serves as a capacitance controller at both sides of the lower portion of the gate electrode. Thus the parasitic capacitance between the gate electrode and substrate can be minimized. Accordingly, the time delay, as an inherent characteristic of the semiconductor device, can be shortened.

**[0190]** Finally, although the present invention has been described above in connection with the preferred embodiments thereof, the present invention is not limited as will be apparent to those skilled in the art. Rather, various changes to and modifications of these embodiments are within the true spirit and scope of the present

invention as hereinafter claimed.